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In the Claims:

Claims 1-29 (Canceled).

30. (Currently amended) A content addressable memory (CAM) array, comprising:

a first match line segment associated with a first row of CAM cells in the CAM array;

an inverter having an input electrically coupled to said first match line segment; and

a match line precharge support circuit electrically connected to said first match line segment and comprising a first PMOS transistor, said first PMOS transistor having a gate terminal electrically coupled to an output of said inverter, a first current carrying terminal that is electrically coupled to said first match line segment and a second current carrying terminal that is electrically coupled to a power supply line.

31. (Original) The CAM array of Claim 30, wherein said match line precharge support circuit further comprises:

a second normally-on PMOS transistor having a first current carrying terminal that is electrically connected to the second current carrying terminal of the first PMOS transistor and a second current carrying terminal that is electrically connected to the power supply line.

32. (Original) The CAM array of Claim 30, wherein said match line precharge support circuit further comprises:

a second normally-on PMOS transistor having a first current carrying terminal that is electrically connected to the first match line segment and a second current carrying terminal that is electrically connected to the first current carrying terminal of said first PMOS transistor.

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33. (Original) The CAM array of Claim 31, wherein said second normally-on PMOS transistor has a gate terminal that is responsive to a P-bias voltage having a magnitude sufficient to maintain said second normally-on PMOS transistor in a linear mode of operation.

34. (Currently amended) The CAM array of Claim 30, wherein a pull-down path of said inverter comprises:

a first NMOS pull-down transistor having a gate terminal that is electrically connected to the input of said inverter and a drain terminal that is electrically connected to the output of said inverter; and

a second NMOS pull-down transistor having a gate terminal that is responsive to an N-bias voltage having a magnitude sufficient to maintain said second NMOS pull-down transistor in a linear mode of operation, a drain terminal that is electrically connected to a source terminal of said first NMOS pull-down transistor and a source terminal that is electrically connected to a reference supply line.

Claims 35-64 (Canceled).

65. (New) A content addressable memory (CAM) array, comprising:
a first match line segment electrically coupled to a first segment of CAM cells within a first row of the CAM array;
an inverter having an input electrically coupled to said first match line segment;
a match line precharge support circuit electrically coupled to said first match line segment, said match line precharge support circuit comprising:
a first PMOS transistor having a gate terminal electrically connected to an output of said inverter and a drain terminal electrically connected to said first match line segment; and
a second PMOS transistor having a drain terminal electrically connected electrically connected to a source terminal of said first PMOS transistor, a source terminal electrically connected to a power supply line and a gate terminal responsive to a P-bias voltage; and
a bias voltage generator that is configured to support generation of the P-bias voltage at a positive voltage level that maintains said second PMOS transistor in a normally-on conductive mode.

66. (New) The CAM array of Claim 65, wherein a pull-down path of said inverter comprises:
a first NMOS pull-down transistor having a gate terminal electrically connected to the input of said inverter and a drain terminal electrically connected to the output of said inverter; and
a second NMOS pull-down transistor having a gate terminal responsive to an N-bias voltage having a magnitude sufficient to maintain said second NMOS pull-down transistor in a linear mode of operation, a drain terminal electrically connected to a source terminal of said first NMOS pull-down transistor and a source terminal electrically connected to a reference supply line.

67. (New) The CAM array of Claim 66, wherein said bias voltage generator is further configured to support generation of the N-bias voltage.

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68. (New) The CAM array of Claim 66, further comprising a third NMOS pull-down transistor having a gate terminal responsive to an evaluation control signal, a drain terminal electrically connected to the drain terminal of said second NMOS pull-down transistor and a source terminal electrically connected to the reference supply line.